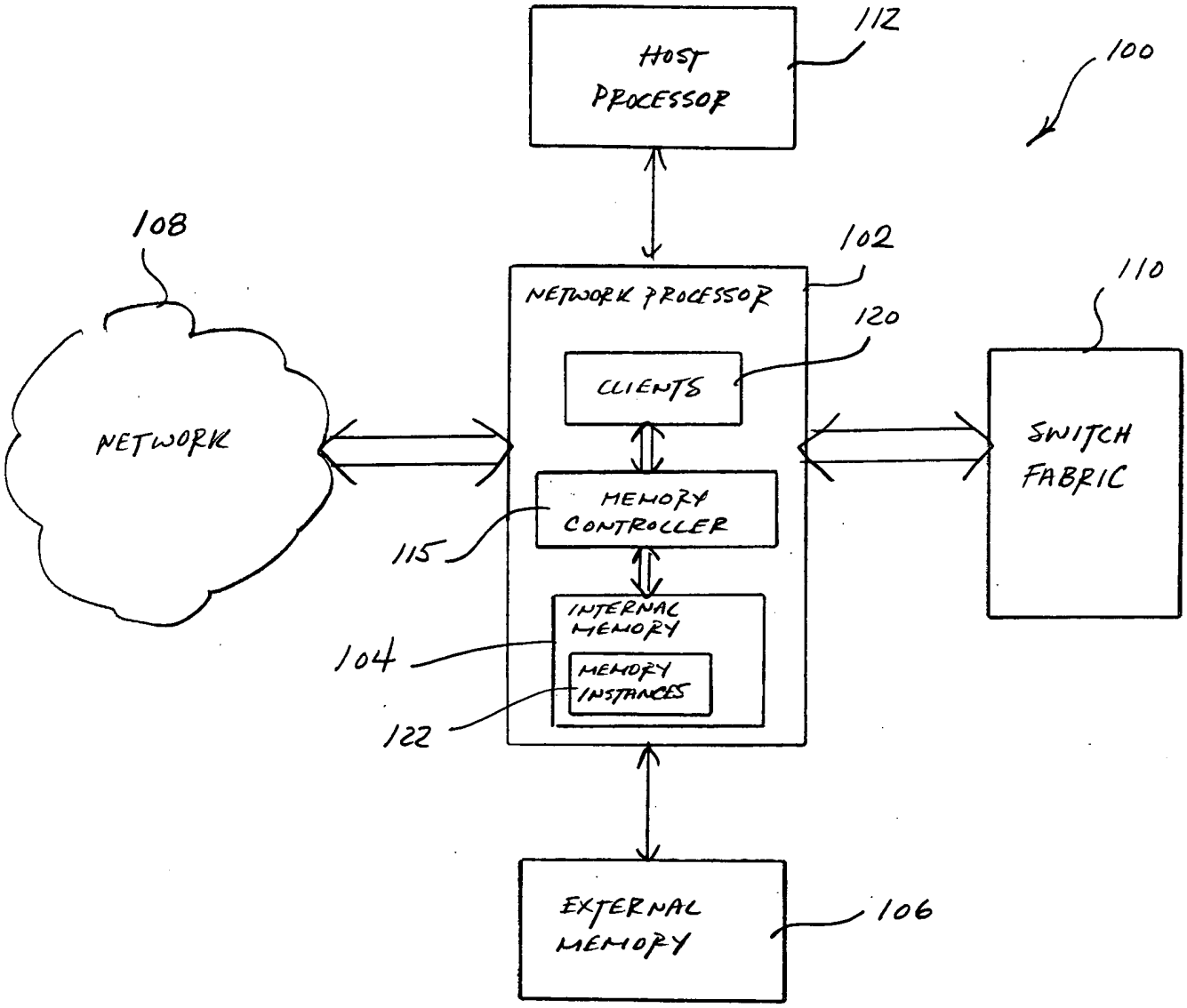
HOST PROCESSOR
112
100
108
102
NETWORK PROCESSOR
110
120
CLIENTS
NETWORK
SWITCH FABRIC
MEMORY CONTROLLER
115
INTERNAL MEMORY
104
MEMORY INSTANCES
122
EXTERNAL MEMORY
106

FIG. 1

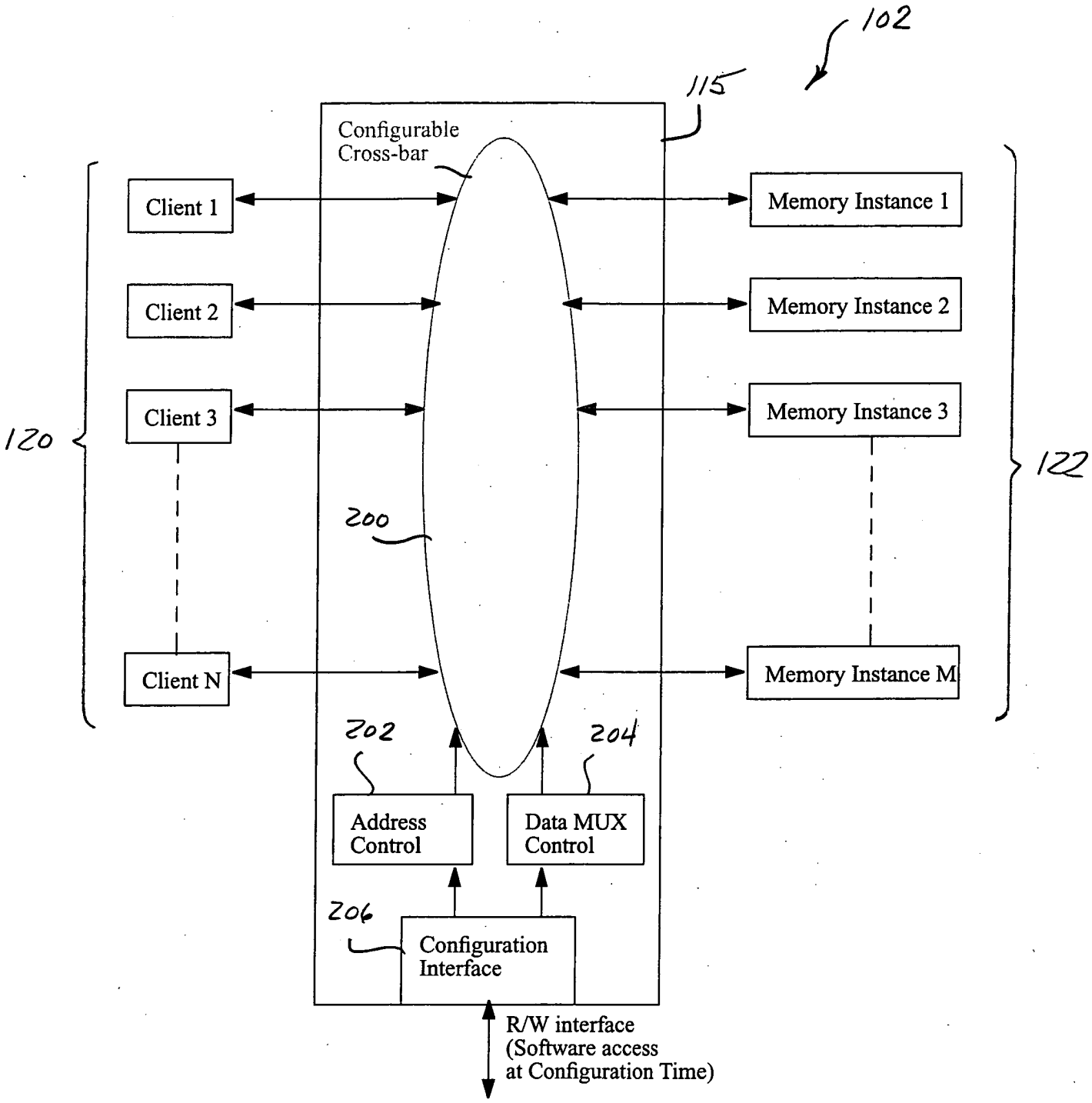
102
115
Configurable
Cross-bar
Client 1
Client 2
Client 3
Client N
120
Memory Instance 1
Memory Instance 2
Memory Instance 3
Memory Instance M
122
200
202
204
Address
Control
Data MUX
Control
206
Configuration
Interface
R/W interface
(Software access
at Configuration Time)

FIG. 2

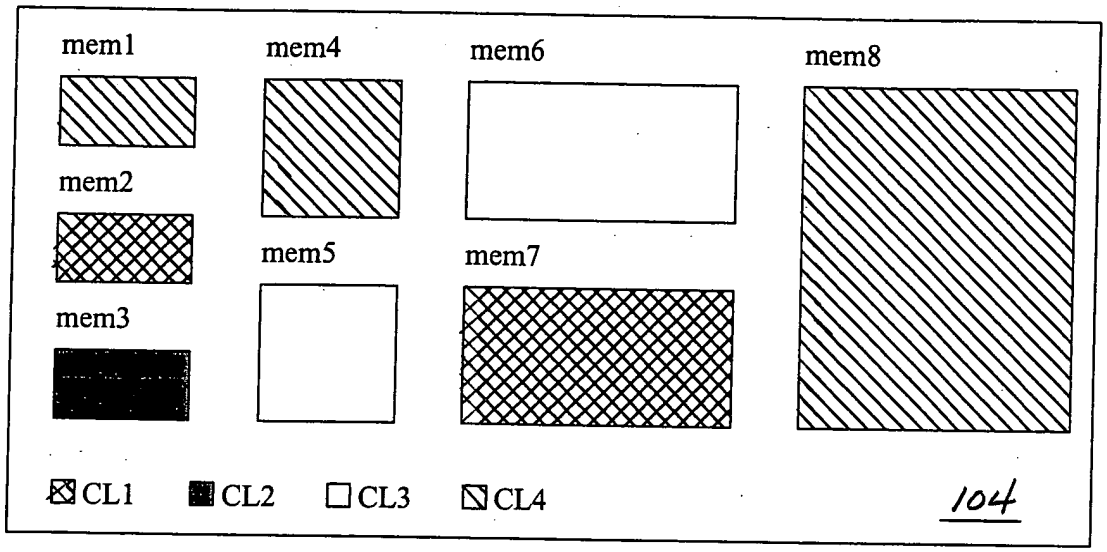
mem1
mem4
mem6
mem8
mem2
mem5
mem7
mem3
CL1
CL2
CL3
CL4
104

FIG. 3A

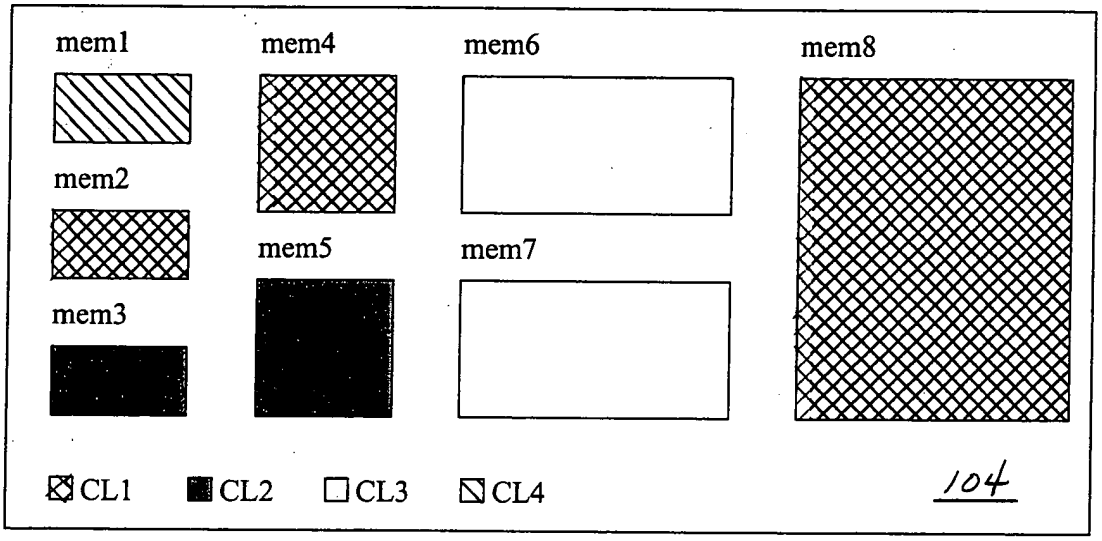
mem1
mem4
mem6
mem8
mem2
mem5
mem7
mem3
CL1
CL2
CL3
CL4
104

FIG. 3B

Memory	Configured Capacity	W rd Addressing Range [19:0]		Address Dec der Value [6:0]	Address Mask Bits [6:0]	Relevant Bits
Mem1	1MB	00000h	3FFFFh	7'b00x_xxxx	7'b001_1111	[19:18]
Mem2	1MB	40000h	7FFFFh	7'b01x_xxxx	7'b001_1111	[19:18]
Mem3	512KB	80000h	9FFFFh	7'b100_xxxx	7'b000_1111	[19:17]
Mem4	512KB	A0000h	BFFFFh	7'b101_xxxx	7'b000_1111	[19:17]
Mem5	256KB	C0000h	CFFFFh	7'b110_0xxx	7'b000_0111	[19:16]
Mem6	128KB	D0000h	D7FFFh	7'b110_10xx	7'b000_0011	[19:15]
Mem7	128KB	D8000h	DFFFFh	7'b110_11xx	7'b000_0011	[19:15]
Mem8	64KB	E0000h	E3FFFh	7'b111_000x	7'b000_0001	[19:14]
Mem9	32KB	E4000h	E5FFFh	7'b111_0010	7'b000_0000	[19:13]

FIG. 4A

Memory Size	Mask bits [6:0]
1MB	7'b001_1111
512KB	7'b000_1111
256KB	7'b000_0111
128KB	7'b000_0011
64KB	7'b000_0001
32KB	7'b000_0000

FIG. 4B

No. Of Bits	Description
[6:0]	Address DecoderValue for a particular internal memory instance.
[6:0]	Address Mask Value as mentioned in the above table, depending on the memory instance size.
[4:0]	Master client for the memory instance. "00001" for CL1..... "10100" for CL20.

FIG. 4C

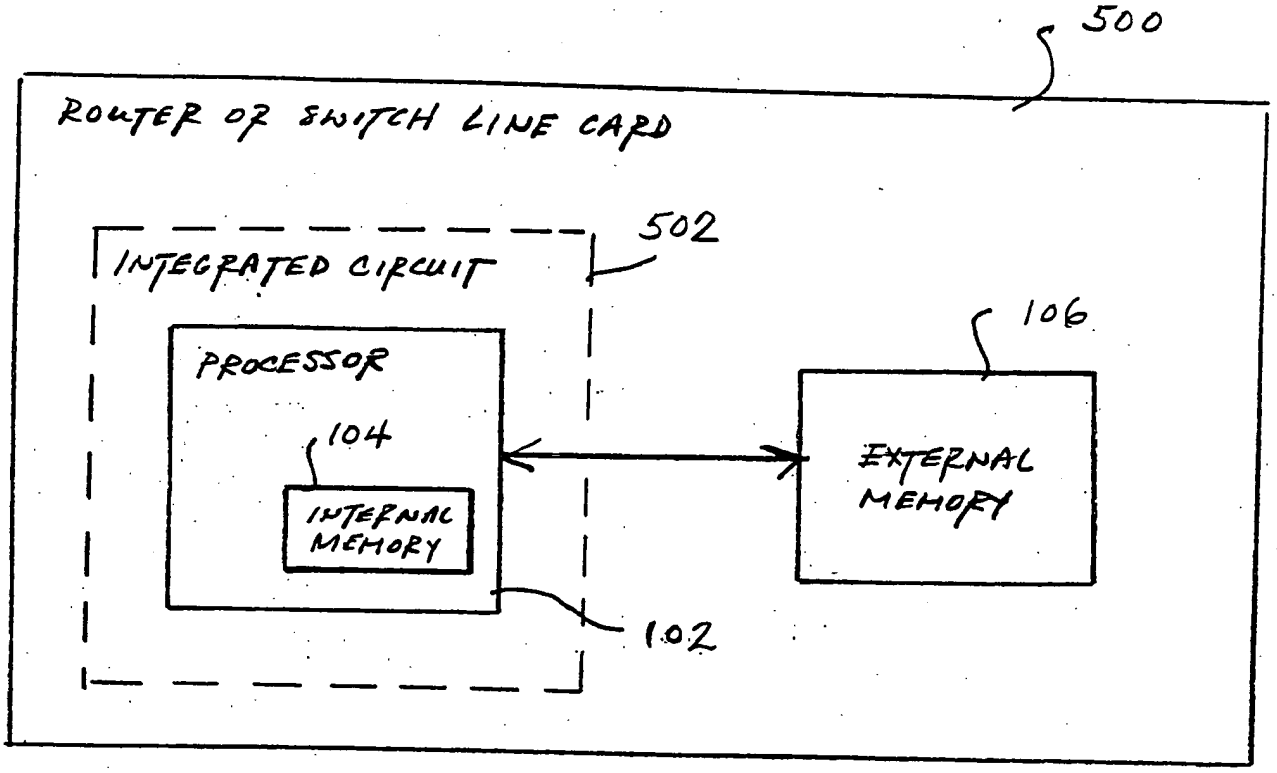
500
ROUTER OR SWITCH LINE CARD
502
INTEGRATED CIRCUIT
106
PROCESSOR
104
INTERNAL MEMORY
EXTERNAL MEMORY
102

FIG. 5